In The Claims:

Claim 1 (Currently amended) A buried bit line formed in a substrate of a semiconductor device, comprising

a shallow doped region, disposed in the substrate; and

a deep doped region, disposed in the substrate under a part of the shallow doped region, a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein dopant concentrations in the deep doped region and the shallow doped region are about the same, and the shallow doped region and the deep doped region together serve as a buried bit line of the memory device.

Claim 2 (Original) The buried bit line of claim 1, wherein forming the shallow doped region and the deep doped region comprises:

forming a patterned mask layer on a substrate;

performing a first doping in the substrate not covered by the mask layer to form the shallow doped region, using the mask layer as a mask;

forming a liner layer with a predetermined thickness on at least a side surface of the mask layer; and

performing a second doping in the substrate not covered by the mask layer and the liner layer to form a deep doped region, using the liner layer and the mask layer as a mask.

Claim 3 (Original) The buried bit line of claim 2, wherein the mask layer comprises a photoresist material, polysilicon or a dielectric material.

Claim 4 (Currently amended) The buried bit line of claim 2, wherein the liner layer comprises a ~~high molecular weight material~~ polymer layer formed by plasma enhanced chemical vapor deposition.

Claim 5 (Original) The buried bit line of claim 2, wherein an implantation energy for forming the deep doped region is about 50 KeV to 120 KeV and an implantation energy for forming the shallow doped region is about 40 KeV to 80 KeV.

Claim 6 (Cancelled)

Claim 7 (Original) The buried bit line of claim 1, wherein a dopant concentration in the shallow doped region is about $10^{21}/cm^3$ to $10^{22}/cm^3$.

Claim 8 (Currently amended) The ~~method~~ buried bit line of claim 5, wherein a dopant concentration in the deep doped region is about $10^{21}/cm^3$ to $10^{22}/cm^3$.

Claims 9-16 (withdrawn)

Claim 17 (Currently amended) A memory device, comprising:

a substrate;

a gate, disposed on a part of the substrate;

a gate oxide layer, disposed between the substrate and the gate;

a shallow doped region, disposed in the substrate beside both sides of the gate; and

a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein dopant concentrations in the deep doped region and the shallow doped region are about the same, and the shallow doped region and the deep doped region together serve as a buried bit line of the memory device.

Claim 18 (Original) The memory device of claim 17, wherein forming the shallow doped region and the deep doped region further comprises:

forming a patterned mask layer on the substrate;

performing a first doped region in the substrate not covered by the mask layer to form the shallow doped region;

forming a liner layer with predetermined thickness on at least a side surface of the mask layer; and

performing a second doped region in the substrate not covered by the liner layer and the mask layer to form a deep doped region.

Claim 25 (Previously Added) The memory device of claim 18, wherein the mask layer is formed with a photoresist material, polysilicon, or a dielectric material.

Claim 26 (Previously Added) The memory device of claim 18, wherein the liner layer comprises a ~~high molecular weight material~~ polymer layer formed by plasma enhanced chemical vapor deposition.

Claim 27 (Previously Added) The memory device of claim 18, wherein the deep doped region is formed with an implantation energy of about 50 KeV to 120 KeV and the shallow doped region is formed with an implantation energy of about 40 KeV to 80 KeV.

Claim 28 (Previously Added) The memory device of claim 18, wherein dopant concentrations in the deep doped region and in the shallow doped region are about the same.

Claim 29 (Previously Added) The memory device of claim 18, wherein a dopant concentration in the deep doped region is about $10^{21}/cm^3$ to $10^{22}/cm^3$

Claim 30 (Previously Added) The memory device of claim 18, wherein a dopant concentration in the shallow doped region is about $10^{21}/cm^3$ to $10^{22}/cm^3$.

Claim 31 (New added) A silicon nitride memory device, comprising:

a substrate;

a shallow doped region, disposed in the substrate;

a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein dopant concentrations in the deep doped region and the shallow doped region are about the same, and the shallow doped region and the deep doped region together serve as a buried bit line;

an electron trapping layer containing a silicon nitride layer, disposed on the substrate; and

a word line, covering the electron trapping layer and across the buried bit line.

Claim 32 (New added) The silicon nitride memory device of claim 1, wherein the electron trapping layer comprises a first silicon oxide and a second silicon oxide layer on and under the silicon nitride layer.